CLAIMS

Although a preferred embodiment of the present invention has been illustrated in the accompanying Drawings and described in the foregoing Detailed Description, it will be understood that the invention is not limited to the embodiments disclosed, but is capable of numerous rearrangements, modifications, and substitutions without departing from the spirit of the invention as set forth and defined by the following claims.

What is claimed is:

1. A thin film capacitor/inductor/interconnect method comprising:

(1) thinly metalizing a substrate with a lower electrode and interconnect layer formed on said thin film hybrid substrate, said layer further comprising a lower adhesive layer and an upper conducting layer having a sum total thickness of less than or equal to 1.5 microns;

(2) applying/imaging photoresist and etching to form metal patterns on said substrate for lower capacitor electrodes and interconnect;

(3) applying a thin dielectric layer to said metal patterns;

(4) applying/imaging photoresist and etching to form contact holes in said dielectric layer and optionally selectively patterning said dielectric layer;

(5) metalizing said substrate to make contact with said lower capacitor electrodes and interconnect;

(6) applying/imaging photoresist and etching to form patterns for upper capacitor electrodes, inductors, and/or interconnect conductors;

(7) optionally forming resistor elements by applying/imaging photoresist and etching a resistor layer on said substrate;

wherein

said upper conducting layer is approximately 0.25 microns thick.

2. The thin film hybrid substrate method of Claim 1, wherein said lower adhesive layer is approximately 0.03 to 0.05 microns thick.

3. The thin film hybrid substrate method of Claim 1, wherein said lower adhesive layer comprises chrome.

4. The thin film hybrid substrate method of Claim 1, wherein said lower adhesive layer comprises titanium.

5. The thin film hybrid substrate method of Claim 1, wherein said lower adhesive layer comprises titanium-tungsten.

6. The thin film hybrid substrate method of Claim 1, wherein said upper conducting layer comprises silver.

7. The thin film hybrid substrate method of Claim 1, wherein said upper conducting layer comprises aluminum.

8. The thin film hybrid substrate method of Claim 1, wherein said upper conducting layer comprises gold.

9. The thin film hybrid substrate method of Claim 1, wherein said upper conducting layer comprises copper.

10. The thin film hybrid substrate method of Claim 1, wherein said lower electrode and interconnect layer further comprises silver.

11. The thin film hybrid substrate method of Claim 1, wherein said lower electrode and interconnect layer further comprises aluminum.

12. The thin film hybrid substrate method of Claim 1, wherein said lower electrode and interconnect layer further comprises gold.

13. The thin film hybrid substrate method of Claim 1, wherein said lower electrode and interconnect layer further comprises copper.

14. The thin film hybrid substrate method of Claim 1, wherein said lower electrode and interconnect layer is selected from the group consisting of tantalum, tungsten, titanium, nickel, molybdenum, platinum, palladium, and chromium.

15. The thin film hybrid substrate method of Claim 1, wherein said dielectric layer is selectively patterned.

16. The thin film hybrid substrate method of Claim 1, wherein said dielectric layer further comprises silicon nitride.

17. The thin film hybrid substrate method of Claim 1, wherein said dielectric layer further comprises silicon dioxide.

18. The thin film hybrid substrate method of Claim 1, wherein said dielectric layer further comprises silicon oxynitride.

19. The thin film hybrid substrate method of Claim 1, wherein said dielectric layer further comprises aluminum oxide.

20. The thin film hybrid substrate method of Claim 1, wherein said dielectric layer further comprises tantalum pentoxide.

21. The thin film hybrid substrate method of Claim 1, wherein said dielectric layer further comprises a ferroelectric material.

22. The thin film hybrid substrate method of Claim 21, wherein said ferroelectric material is $BaTiO_3$.

23. The thin film hybrid substrate method of Claim 21, wherein said ferroelectric material is $SrTiO_3$.

24. The thin film hybrid substrate method of Claim 21, wherein said ferroelectric material is $PbZrO_3$.

25. The thin film hybrid substrate method of Claim 21, wherein said ferroelectric material is $PbTiO_3$.

26. The thin film hybrid substrate method of Claim 21, wherein said ferroelectric material is $LiNbO_3$.

27. The thin film hybrid substrate method of Claim 21, wherein said ferroelectric material is $Bi_{14}Ti_3O_{12}$.

28. The thin film hybrid substrate method of Claim 1, wherein said dielectric layer further comprises polyimide.

29. The thin film hybrid substrate method of Claim 1, wherein said dielectric layer further comprises benzocyclobutene.

30. The thin film hybrid substrate method of Claim 1, wherein said substrate material is selected from the group consisting of alumina, beryllium oxide, fused silica, aluminum nitride, sapphire, ferrite, diamond, LTCC, and glass.

31. The capacitor/inductor/interconnect product of the thin film fabrication method comprising:

(1) thinly metalizing a substrate with a lower electrode and interconnect layer formed on said thin film hybrid substrate, said layer further comprising a lower adhesive layer and an upper conducting layer having a sum total thickness of less than or equal to 1.5 microns;

(2) applying/imaging photoresist and etching to form metal patterns on said substrate for lower capacitor electrodes and interconnect;

(3) applying a thin dielectric layer to said metal patterns;

(4) applying/imaging photoresist and etching to form contact holes in said dielectric layer and optionally selectively patterning said dielectric layer;

(5) metalizing said substrate to make contact with said lower capacitor electrodes and interconnect;

(6) applying/imaging photoresist and etching to form patterns for upper capacitor electrodes, inductors, and/or interconnect conductors;

(7) optionally forming resistor elements by applying/imaging photoresist and etching a resistor layer on said substrate;

wherein

said upper conducting layer is approximately 0.25 microns thick.

32. The capacitor/inductor/interconnect product of Claim 31, wherein said lower adhesive layer is approximately 0.03 to 0.05 microns thick.

33. The capacitor/inductor/interconnect product of Claim 31, wherein said lower adhesive layer comprises chrome.

34. The capacitor/inductor/interconnect product of Claim 31, wherein said lower adhesive layer comprises titanium.

35. The capacitor/inductor/interconnect product of Claim 31, wherein said lower adhesive layer comprises titanium-tungsten.

36. The capacitor/inductor/interconnect product of Claim 31, wherein said upper conducting layer comprises silver.

37. The capacitor/inductor/interconnect product of Claim 31, wherein said upper conducting layer comprises aluminum.

38. The capacitor/inductor/interconnect product of Claim 31, wherein said upper conducting layer comprises gold.

39. The capacitor/inductor/interconnect product of Claim 31, wherein said upper conducting layer comprises copper.

40. The capacitor/inductor/interconnect product of Claim 31, wherein said lower electrode and interconnect layer further comprises silver.

41. The capacitor/inductor/interconnect product of Claim 31, wherein said lower electrode and interconnect layer further comprises aluminum.

42. The capacitor/inductor/interconnect product of Claim 31, wherein said lower electrode and interconnect layer further comprises gold.

43. The capacitor/inductor/interconnect product of Claim 31, wherein said lower electrode and interconnect layer further comprises copper.

44. The capacitor/inductor/interconnect product of Claim 31, wherein said lower electrode and interconnect layer is selected from the group consisting of tantalum, tungsten, titanium, nickel, molybdenum, platinum, palladium, and chromium.

45. The capacitor/inductor/interconnect product of Claim 31, wherein said dielectric layer is selectively patterned.

46. The capacitor/inductor/interconnect product of Claim 31, wherein said dielectric layer further comprises silicon nitride.

47. The capacitor/inductor/interconnect product of Claim 31, wherein said dielectric layer further comprises silicon dioxide.

48. The capacitor/inductor/interconnect product of Claim 31, wherein said dielectric layer further comprises silicon oxynitride.

49. The capacitor/inductor/interconnect product of Claim 31, wherein said dielectric layer further comprises aluminum oxide.

50. The capacitor/inductor/interconnect product of Claim 31, wherein said dielectric layer further comprises tantalum pentoxide.

51. The capacitor/inductor/interconnect product of Claim 31, wherein said dielectric layer further comprises a ferroelectric material.

52. The capacitor/inductor/interconnect product of Claim 51, wherein said ferroelectric material is $BaTiO_3$.

53. The capacitor/inductor/interconnect product of Claim 51, wherein said ferroelectric material is $SrTiO_3$.

54. The capacitor/inductor/interconnect product of Claim 51, wherein said ferroelectric material is $PbZrO_3$.

55. The capacitor/inductor/interconnect product of Claim 51, wherein said ferroelectric material is $PbTiO_3$.

56. The capacitor/inductor/interconnect product of Claim 51, wherein said ferroelectric material is $LiNbO_3$.

57. The capacitor/inductor/interconnect product of Claim 51, wherein said ferroelectric material is $Bi_{14}Ti_3O_{12}$.

58. The capacitor/inductor/interconnect product of Claim 31, wherein said dielectric layer further comprises polyimide.

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59. The capacitor/inductor/interconnect product of Claim 31, wherein said dielectric layer further comprises benzocyclobutene.

60. The capacitor/inductor/interconnect product of Claim 31, wherein said substrate material is selected from the group consisting of alumina, beryllium oxide, fused silica, aluminum nitride, sapphire, ferrite, diamond, LTCC, and glass.

61. A power supply bypass/decoupling/filter network system fabricated using array elements comprising integrated capacitors, inductors, and/or interconnects formed on a thin film hybrid substrate system comprising:

(a) a thin film hybrid substrate;

(b) a lower electrode and interconnect layer formed on said thin film hybrid substrate, said layer further comprising a lower adhesive layer and an upper conducting layer having a sum total thickness less than or equal to 1.5 microns.

(c) a dielectric layer deposited on top of the said patterned lower electrode and interconnect layer; and

(d) an upper electrode layer formed on said dielectric layer;

wherein

said upper conducting layer is approximately 0.25 microns thick.

62. A phased antenna array system fabricated using array elements comprising integrated capacitors, inductors, and/or interconnects formed on a thin film hybrid substrate system comprising:

(a) a thin film hybrid substrate;

(b) a lower electrode and interconnect layer formed on said thin film hybrid substrate, said layer further comprising a lower adhesive layer and an upper conducting layer having a sum total thickness less than or equal to 1.5 microns.

(c) a dielectric layer deposited on top of the said patterned lower electrode and interconnect layer; and

(d) an upper electrode layer formed on said dielectric layer;

wherein

said upper conducting layer is approximately 0.25 microns thick.

63. The phased antenna array system of Claim 62, wherein said array elements further comprise an inductor/capacitor bypass/decoupling/filter network fabricated using said integrated capacitors, inductors, and/or interconnects of Claim 61.

64. The phased antenna array system of Claim 62, wherein said array elements are active.

65. The phased antenna array system of Claim 64, wherein said array elements further comprise an inductor/capacitor bypass/decoupling/filter network fabricated using said integrated capacitors, inductors, and/or interconnects of Claim 61.

66. The phased antenna array system of Claim 62, wherein said array elements are passive.

67. The phased antenna array system of Claim 66, wherein said array elements further comprise an inductor/capacitor bypass/decoupling/filter network fabricated using said integrated capacitors, inductors, and/or interconnects of Claim 61.